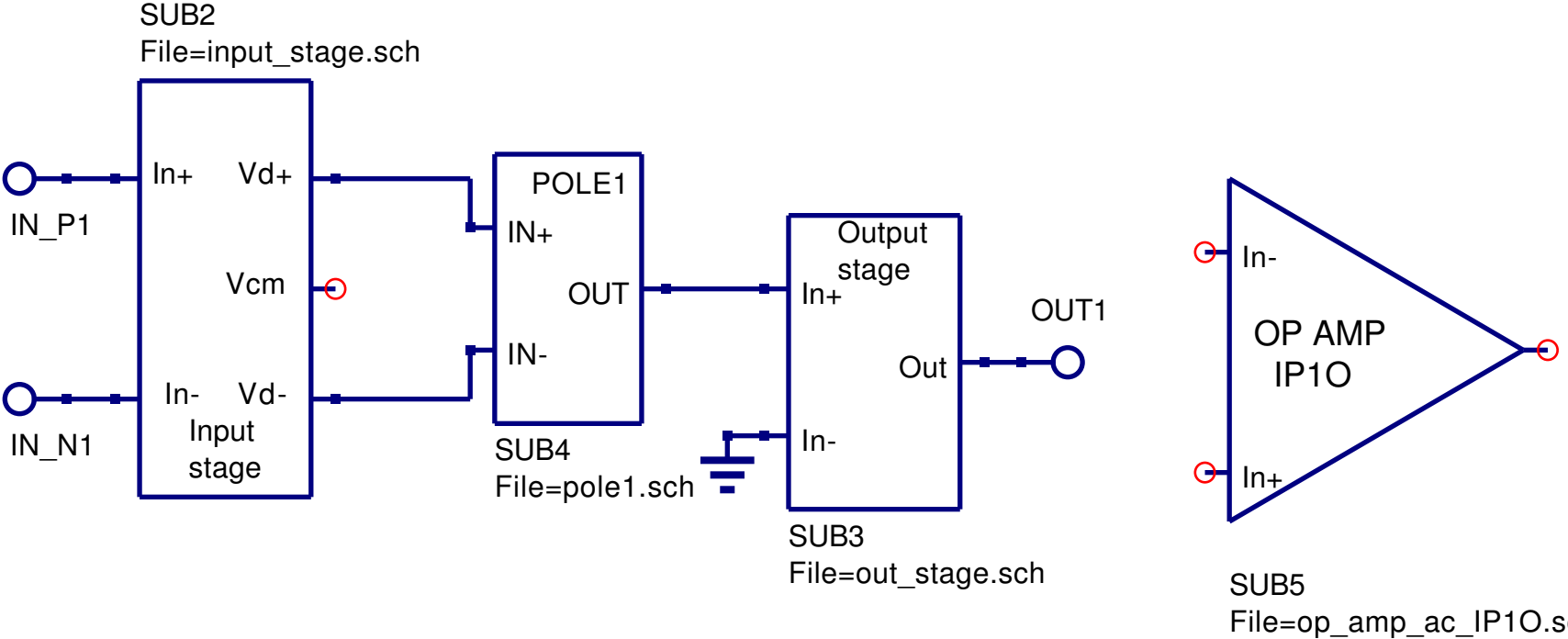
SUB2
File=input_stage.sch
In+
Vd+
Vcm
In-
Vd-
Input
stage
IN_P1
IN_N1
POLE1
IN+
OUT
IN-
SUB4
File=pole1.sch
Output
stage
In+
Out
In-
OUT1
SUB3
File=out_stage.sch
In-
OP AMP
IP1O
In+
SUB5
File=op_amp_ac_IP1O.sch